HIGHLY SCALABLE METHODS AND APPARATUS FOR MULTIPLEXING SIGNALS

FIELD OF THE INVENTION

The present invention relates generally to integrated circuit design, and more particularly to methods and apparatus for multiplexing signals.

BACKGROUND OF THE INVENTION

A need may arise in many data, communications or other similar systems to switch between multiple asynchronous clocks, data signals or the like. Such switching typically is accomplished via multiplexers.

Many conventional multiplexer systems generate spurious signals or "glitches" at multiplexer outputs when the multiplexer systems switch between output signals. Glitches may generate false logic states within an integrated circuit, and may damage sensitive circuit devices. High frequency circuits are especially vulnerable as they may generate large, high frequency glitches that may mix to produce undesirable input or output tones.

Numerous approaches have been proposed for reducing glitches during switching, such as allowing a predetermined time to elapse after switching before a new signal is output (e.g., so that all output nodes of a multiplexer have time to stabilize), or using cascaded edge triggered latches to minimize meta-stability in a data path. Other proposed approaches that relate specifically to switching between clock signals include pulling an output node to a predetermined state in between clock transitions (regardless of the previous state of the output node), requiring a selected clock signal to reach a

predetermined logic state before allowing switching, or using edge detection to detect a change in the selection of a specific clock. However, such approaches may result in substantial switching delays, be difficult or expensive to implement and/or fail as the frequency of signal selection increases.

Accordingly, a need exists for improved methods and apparatus for multiplexing signals.

SUMMARY OF THE INVENTION

In a first aspect of the invention, a first method is provided that includes providing a plurality of select signals and a plurality of input signals for input by a multiplexer. Each select signal is adapted to cause the multiplexer to select a different one of the plurality of input signals for output by the multiplexer when the select signal is in a first logic state. The first method further includes preventing a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state.

In a second aspect of the invention, a second method is provided that includes providing a plurality of select signals and a plurality of clock input signals for input by a multiplexer. Each select signal is adapted to cause the multiplexer to select a different one of the plurality of clock input signals for output by the multiplexer when the select signal is in a first logic state. The second method further includes the steps of (1) preventing a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state;

and (2) preventing the first of the select signals from reaching the multiplexer until after a rising edge and a falling edge of a corresponding first of the clock input signals. Numerous other aspects are provided, as are systems and apparatus in accordance with these and other aspects of the invention.

Other features and aspects of the present invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a multiplexer system provided in accordance with the present invention.

FIG. 2 is a schematic diagram of an exemplary embodiment of the synchronization and one-shot detection (SOSD) circuit of FIG. 1.

FIG. 3 illustrates the switching characteristics of the multiplexer of FIG. 1 without the SOSD circuit of FIG. 1.

FIG. 4 illustrates the switching characteristics of the multiplexer of FIG. 1 with the SOSD circuit of FIG. 1.

DETAILED DESCRIPTION

FIG. 1 is a schematic diagram of a multiplexer system 100 provided in accordance with the present invention. With reference to FIG. 1, the multiplexer system 100 includes a multiplexer 102 coupled to a select control circuit 104.

The multiplexer 102 may comprise any conventional multiplexing circuit that employs a plurality of select

signals to selectively output one of a plurality of input signals provided to the multiplexer 102. For example, in the embodiment of FIG. 1, the multiplexer 102 comprises (1) a plurality of data input nodes 106a-d adapted to receive data input signals (e.g., clock signals such as Clk_1, Clk_2, Clk_3 and Clk_4, respectively, or other data input signals); (2) a plurality of select nodes 108a-d adapted to cause the multiplexer 102 to select one of the data input signals provided to one of the data input nodes 106a-d in response to "synchronized" select signals C1-C4 (as described below); and (3) an output node 110 adapted to output the selected data input signal (e.g., as Clk_Out). Other numbers of data input, select and/or output nodes may be employed.

Each select node 108a-d corresponds to a different one of the plurality of data input nodes 106a-d. For example, the first select node 108a may correspond to the first input node 106a, the second select node 108b may correspond to the second input node 106b, etc. As will be described further below, when one of the select nodes 108a-d of the multiplexer 102 receives a predetermined logic state signal (e.g., a high logic state signal) from the select control circuit 104, the multiplexer 102 outputs (via the output node 110) the data signal provided to the data input node 106a-d that corresponds to the select node 108a-d that received the predetermined logic state signal. For example, in one embodiment, if the select control logic 104 outputs logic states 1,0,0,0 to the select nodes 108a-d, respectively, the multiplexer 102 outputs (via the output node 110) the data input signal provided to the first data input node 106a (e.g., clk_1). Likewise, if the select control logic 104 outputs logic states 0,1,0,0 to

the select nodes 108a-d, respectively, the multiplexer 102 outputs the data input signal provided to the second data input node 106b (e.g., clk_2), etc.

The select control circuit 104 includes a decoder 112 coupled to a synchronization and one-shot detection circuit 114. The decoder 112 receives a plurality of control signals 116a-b (e.g., Ctrl1 and Ctrl2) and generates a plurality of "unsynchronized" select signals E1-E4. Each unsynchronized select signal E1-E4 is synchronized by the synchronization and one-shot detection circuit 114 to form a synchronized select signal C1-C4, respectively, as described further below. The decoder 112 may comprise any conventional decoding logic. In the embodiment shown, the decoder 112 comprises a 2-to-4 decoder (e.g., as the multiplexer 102 comprises a 4-to-1 multiplexer), although other decoder logic and/or multiplexer sizes may be employed.

The synchronization and one-shot detection circuit 114 includes logic that is adapted to (1) receive the unsynchronized select signals E1-E4 from the decoder 112; (2) ensure that only one of the unsynchronized select signals E1-E4 is in a predetermined logic state (e.g., a high logic state); (3) synchronize each unsynchronized select signals E1-E4 via the clock signals Clk_1-Clk_4, respectively, so as to generate the synchronized select signals C1-C4; and (4) provide the synchronized select signals C1-C4 to the select nodes 108a-d, respectively, of the multiplexer 102. An exemplary embodiment of the synchronization and one-shot detection circuit 114 is described below with reference to FIG. 2.

FIG. 2 is a schematic diagram of an exemplary embodiment of the synchronization and one-shot detection

(SOSD) circuit 114 of FIG. 1. With reference to FIG. 2, the SOSD circuit 114 comprises a plurality of sub-circuits 202a-d each adapted to generate a different one of the synchronized select signals C1-C4 from the unsynchronized select signals E1-E4. For example, the first sub-circuit 202a includes a NOR gate 204a adapted to receive the synchronized select signals C2-C4 that are fed back to the SOSD circuit 114 as shown in FIG. 1 and to perform a NOR operation on the select signals C2-C4. The result of the NOR operation, which will be a high logic state only if the select signals C2-C4 are all in a low logic state, is output to a NAND gate 206a along with the asynchronous select signal E1.

In response to the output of the NOR gate 204a and the asynchronous select signal E1, the NAND gate 206a generates an output that is latched via a first latch 208a (e.g., a D-type latch) in response to a rising edge of the first clock signal Clk_1 and a second latch 210b in response to a falling edge of the first clock signal Clk_1. Note that if the asynchronous select signal E1 is high, indicating that the multiplexer 102 is to output the first clock signal Clk_1, the high logic state may not pass through the NAND gate 206a to the latches 208a, 210a unless the synchronized clock signals C2-C4 are all in a low logic state. Further, once the asynchronous select signal E1 has passed through the NAND gate 206a, it is unable to reach the multiplexer 102 (as the first synchronized select signal C1) until after both a rising and a falling edge of the first clock signal Clk_1. In this manner, the sub-circuit 202a ensures that the first synchronous select signal C1 (1) does not reach the multiplexer 102 unless the remaining synchronous select signals C2-C4 are in a low

logic state; and (2) is synchronized with the first clock signal Clk_1. The sub-circuits 202b-202d employ NOR gates 204b-d, NAND gates 206b-d and latches 208b-d, 210b-d, respectively, to similarly ensure that each synchronous select signal C2-C4 (1) does not reach the multiplexer 102 unless the remaining synchronous select signals are in a low logic state; and (2) is synchronized with its respective clock signal Clk2-Clk4.

Through use of the SOSD circuit 114, erroneous enabling of multiple clock signals via the multiplexer 102 is prevented, as only one select signal C1-C4 at a time may reach the multiplexer 102. Likewise, because each select signal C1-C4 is synchronized to a respective clock signal Clk_1-Clk_4, data paths through the multiplexer 102 are enabled/disabled in a substantially glitch-less manner.

To illustrate operation of the inventive multiplexer system 100 of FIGS. 1 and 2, operation of the multiplexer 102 with and without the SOSD circuit 114 was simulated (e.g., using 10S0 SOI CMOS technology available from International Business Machines Corporation). Specifically, FIG. 3 illustrates the switching characteristics of the multiplexer 102 (FIG. 1) without the SOSD circuit 114 and with the first clock (Clk_1) operating at 5 GHz, the second clock (Clk_2) operating at 1 GHz, the third clock (Clk_3) operating at 500 MHz and the fourth clock (Clk_4) operating at 333 MHz. As shown by the output of the multiplexer 102 (Clk_Out), at time T1 control signals 116a-b (Ctrl1 and Ctrl2) are both high, and the first clock Clk_1 is output from the multiplexer 102. At time T2 (and as indicated by reference numeral 302), the second control signal 116b (Ctrl2) is switched low so that the multiplexer 102 switches from outputting the first

clock signal Clk_1 to outputting the fourth clock signal Clk_4. As indicated by reference numeral 304, absent the SOSD circuit 114, such switching may produce a glitch at the output of the multiplexer 102 (Clk_Out). Similar glitches may be produced when switching between any of the clocks Clk_1-Clk_4. Glitches may generate false logic states within an integrated circuit, and may damage sensitive circuit devices. High frequency circuits are especially vulnerable as they may generate large, high frequency glitches that may mix to produce undesirable input or output tones.

FIG. 4 illustrates the switching characteristics of the multiplexer 102 with the SOSD circuit 114 present. The clock frequencies used to generate the data of FIG. 3 were again employed. As shown by the output of the multiplexer 102 (Clk_Out), at time T1 control signals 116a-b (Ctrl1 and Ctrl2) are both high, and the first clock Clk_1 is output from the multiplexer 102. At time T2 (and as indicated by reference numeral 402), the second control signal 116b (Ctrl2) is switched low so that the multiplexer 102 switches from outputting the first clock signal Clk_1 to outputting the fourth clock signal Clk_4. In contrast to FIG. 3, when the SOSD circuit 114 is employed, such switching does not produce a glitch at the output of the multiplexer 102 (Clk_Out). In fact, glitches are not observed when switching between any of the clocks Clk_1-Clk_4.

The foregoing description discloses only exemplary embodiments of the invention. Modifications of the above disclosed apparatus and methods which fall within the scope of the invention will be readily apparent to those of ordinary skill in the art. For instance, the

present invention may be employed to switch between any type of data signals (e.g., data signals other than clock signals). While the inventive multiplexer system 100 has been described with reference to a 4-to-1 multiplexer (e.g., four data inputs to one output), it will be understood that the invention may be employed with larger or smaller multiplexers, multiple output multiplexers or the like. Larger data selection may be achieved (e.g., merely by increasing the fan in of the NOR gates 204a-d). That is, the inventive multiplexer system 100 is highly scalable. Other types of latches (e.g., edge triggered) may be employed for the latches 208a-d and/or 210a-d.

Accordingly, while the present invention has been disclosed in connection with exemplary embodiments thereof, it should be understood that other embodiments may fall within the spirit and scope of the invention, as defined by the following claims.